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FPGA Implementation of Digital PI Filter and Reset Loop Controller for DPLL

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Abstract

This paper presents implementation of Digital PI (Proportional- Integral) filter on FPGA and reset loop filter for Digital Phase Locked Loops (DPLL). The PI filter is derived from control theory, known as "proportional + integral" action. The proportional controllers are commonly used in industry and it takes control action based on the present control errors. The paper aims to obtain proper FPGA implementation results of Digital PI filter for DPLL and in addition to it, a reset loop filter is designed which involves, damping the filter response to improve the overall locking performance in DPLL. VHDL programming language is used for coding and the software used is Libero ide v9.1. The designed Digital PI filter and reset loop filter or controller in VHDL is verified with FPGA implementation results.

Keywords: Proportional, Integral, Reset Loop filter, VHDL, FPGA, and DPLL.

Introduction

With reference to the previous works [1] and [2], this is the further improvement or work of the paper. DPLL's are used in a lot of electrical engineering technologies. DPLL's are only sustainable in systems that do not change with technology. Since there are very few of these systems, the DPLL can also be unsustainable. Technology is always updating and with newer technologies, different approaches arise to build DPLL's.

Digital implementation of filter is advantageous because in conventional PLL, the loop filter occupies as much as 50% of the chip where as a digital loop filter does not contain any large capacitors, resistors etc and hence, it significantly reduces the overall chip area. In DPLL, the digital filter is based on the difference equation with convergence decided by the coefficients of the equation and phase detector operation is related to the instant of sampling rather than two frequency comparison. Hence DPLL can achieve lock within few cycles.

Digital PI filter

The Digital filter designed consists of two factors such as proportionality (Kp) term and integrator (Ki) term. Proportionality consists of multiplier element and integrator consists of delay and adder element. Kp term is a low pass filter which determines the speed of entire system.

The proportional term produces an output that is proportional to the present error value and it does not consider the past history of errors. The proportional response is obtained by multiplying the current error value by a proportional gain constant called as proportional gain. The Digital IIR low pass filter acts as an integrator, which means continually summing. The integral term K_i responds to accumulated errors from the past. The integral term affects both magnitude of the error and duration of the error. The accumulated error is then multiplied by the integral gain K_i and added to the output. The Fig.1 shows the structure of Digital PI filter

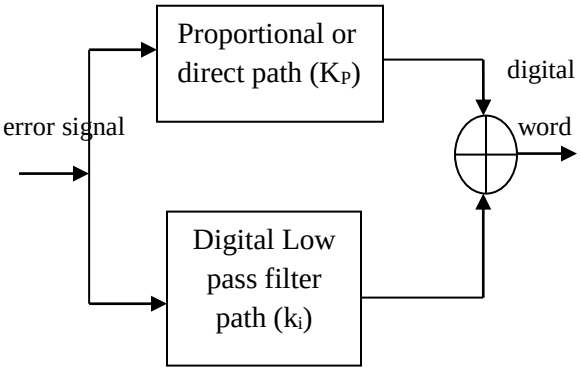

Fig.1: Digital PI filter.

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The DPLL designed for the receiver with Digital PI filter was able to track reference frequency i.e., VCO was able to track and lock on to the reference frequency of 10 KHz range. So, in order to improve loop locking performance another variation of filter is implemented i.e., Reset loop controller.

Reset loop controller or filter

A second variation was made to the designed Digital PI filter, i.e., Sample Reset Loop filter. Introduction of damping factor to the Digital loop filter was made by resetting the Loop filter whenever the output value crosses the limit. Whenever the Loop filter is reset, it takes the new phase error coming out of phase detector and then samples or filters out the phase error in order to improve stability.

Based on the output value of Digital filter, whether it gives positive or negative value, it increments or decrements the accumulator. By following this method the response of the filter is damped to reach stability, so that it retains the response for some time before it samples next successive error signal present at the input. The Fig.2 shows the structure or algorithm for implementing Reset loop filter.

In addition, the filter accumulator width was limited to DAC upper and lower limit. This accumulator value is again compared with outer accumulator for positive or negative value. Whenever it positive, it increments digital word by 1in offset binary, if negative it decrements by1.The initial value of accumulator is set to 512.

PI filter

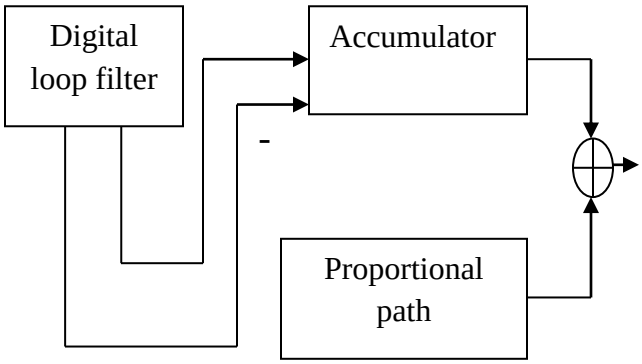

Fig.2: Reset loop filter.

I. FPGA IMPLEMENTATION RESULTS

This section gives FPGA implementation results of Digital PI filter and DPLL results with external VCO and XOR as phase detector, which is an extension of previous work [1] and [2].

Digital PI filter results

A. Digital low pass filter result

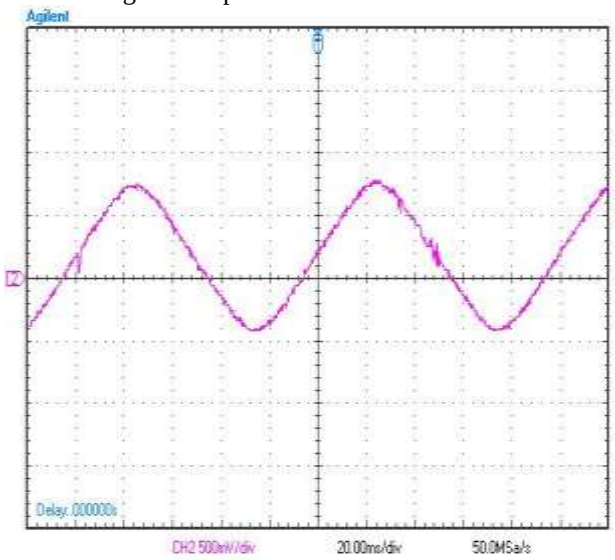

Fig.3: FPGA result of Digital low pass filter path output.

The Fig.3 shows the Digital low pass filter path output which is independent of proportional path. The above filter is designed for a cut off frequency of 10Hz and sampling frequency of 1 KHz.

B. Proportional or direct path controller result

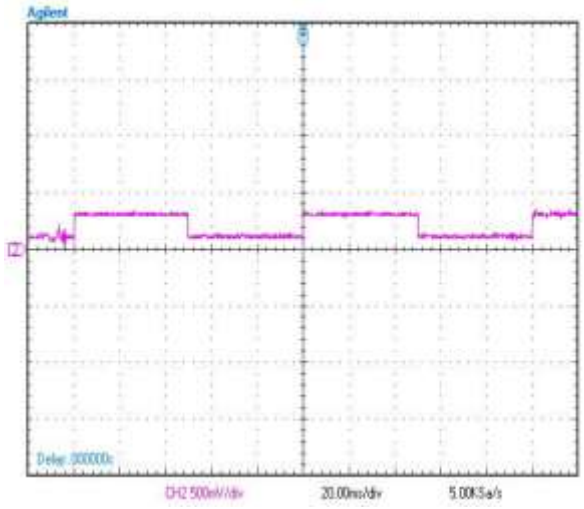

Fig.4: Direct path output of PI filter.

The direct path has a gain value of the inverse power of two. The direct or proportional path multiplies the error signal by gain value which is inverse power of two.

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C. Proportional- Integral filter FPGA results

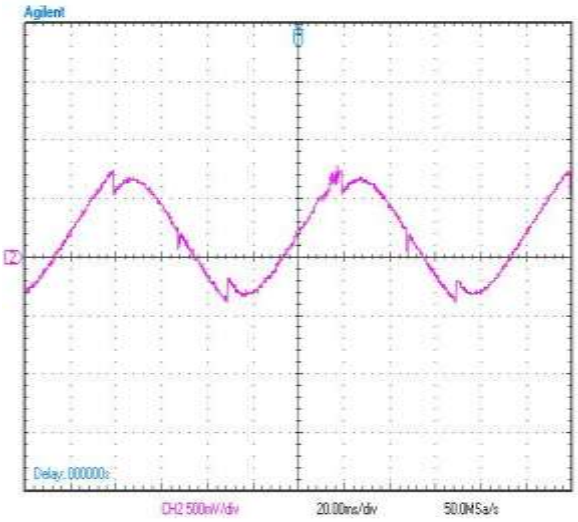

Fig.5: Direct path + low pass filter path output (PI).

The Fig.5 gives addition of both low pass filter path and proportional path.

All the FPGA implementation results obtained, which involves hardware interfacing of ADC, DAC, OP-AMP, BUFFER, from Fig.3 to Fig.5 match the corresponding simulation results in VHDL, done in previous work [1] and [2].

Digital phase detection results with external VCO

A. When there is no input to VCO initially, it will operate at center frequency say fo, then the phase difference between input or reference signal and VCO signal will be approximately 90 degrees which is shown in Fig.6.

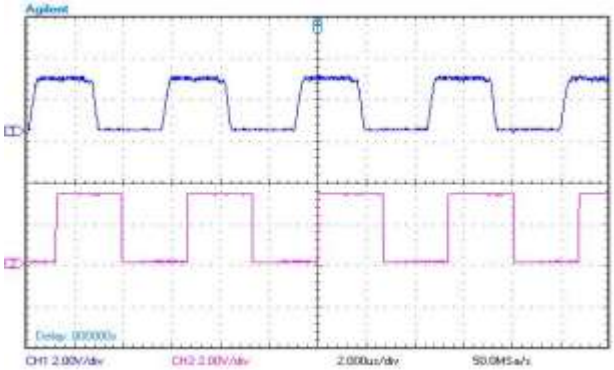

Fig.6: Phase difference between reference and VCO signal is approximately 90 degrees

B. When both the reference signal and VCO signal are out of phase, the phase difference between them will be 180 degrees which is shown in Fig.5.7

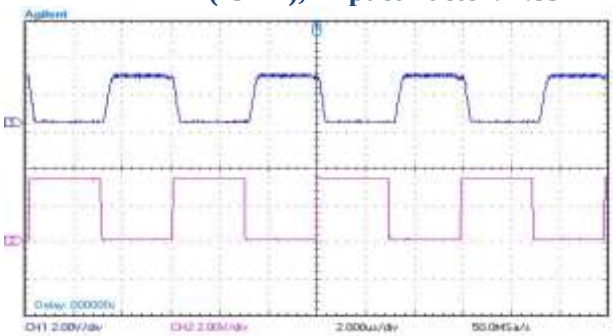

Fig.7: Phase difference between reference and VCO signal is 180 degrees (unlocked condition at 169 KHz).

C. When both the reference and VCO signal are of same phase i.e., it remains in locked condition which is shown in Fig.5.8.

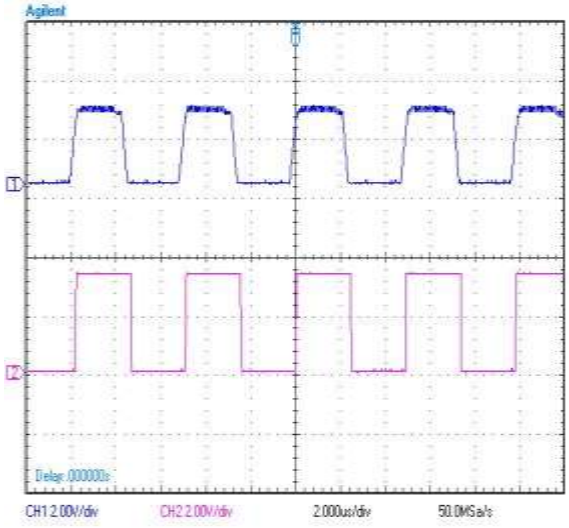

Fig.8: Phase difference between reference and VCO signal is 0 degrees (locked condition at 200 KHz).

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Reset loop filter simulation result

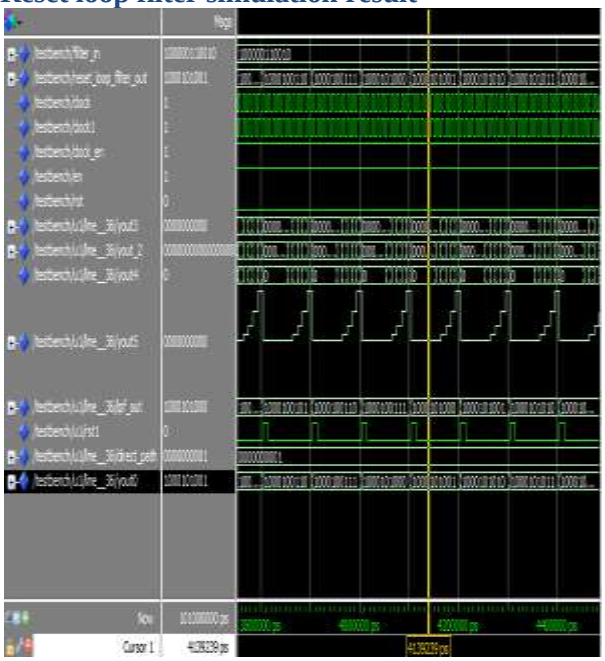

Fig.9: Resetting the Loop filter whenever the output crosses the limit.

The Fig.9 shows the simulation result of Reset Loop filter, which was used to improve the locking performance. Here, the filter output is limited with certain value, whenever the output crosses the limit, Digital Loop controller is reset and then it will take fresh values of phase error, samples and filters out it. Another variation was made by limiting the input value entering into the filter and varying the gain of integral path from 1 to 80.

Conclusion

The paper discusses the verification FPGA implementation results of Digital PI filter with the corresponding VHDL simulation results. The digital phase detection with external VCO for DPLL with hardware implementation is shown with lock and unlock frequencies. In addition to this, in order to improve locking performance a method or variation of PI filter known as Reset loop filter is designed in digital domain and corresponding VHDL simulation results are shown.

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